REMARKS

Claims 29-41 and 44-49, 51-64 are pending in this application. Claims 29, 36 and 44 have been amended. Claims 42, 43 and 50 have been canceled and their limitations have been incorporated in amended independent claims 36 and 44, respectively. No new matter has been introduced. New claims 55-64 have been added to round out the scope of protection afforded by the present invention.

At the outset, Applicant reiterates that the limitation "electropolished patterned metal layer" is simply not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics. The term "electropolished patterned" describes the physical characteristics of the metal layer in amended independent claims 29, 36 and 44. Specifically, the term "electropolished patterned" is a limitation of the metal layer. Claim limitations which confer distinct and defined characteristics of a structure have been analyzed by the Federal Circuit in Hazani v. U.S. Int'l Trade Comm'n, for example. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997). In Hazani, the Federal Circuit specifically emphasized that the claims in question, which were directed to a memory cell comprising a conductive plate having a surface that was "chemically engraved," were "pure product claims" and not product-by-process claims. In arriving at this conclusion, the Federal Circuit reasoned that "Hazani argues that the 'chemically engraved' claims are product-by-process claims. We agree with the respondents, however, that those claims are best characterized as pure product claims, since the 'chemically engraved' limitation, read in context, describes the product more by its structure than by the process used to obtain it." Id. Accordingly, in view of Hazani, the limitation "electropolished patterned metal layer" of amended independent claims 29, 36 and 44 is a structural limitation and not a product-by-process limitation. An "electropolished patterned metal layer," like the "chemically engraved" plate of Hazani, is a *resulting structure* having distinct and defined characteristics and not a product formed by a particular process.

Claims 29-32, 34-39, 41, 44-47 and 49-54 stand rejected under 35 U.S.C. § 103(a) over Dornfest et al. (U.S. Patent No. 6,358,810) ("Dornfest"). This rejection is respectfully traversed.

The claimed invention relates to an electropolished patterned metal layer formed as part of a semiconductor device. As such, amended independent claim 29 recites "an insulating layer provided over said substrate" and "an electropolished patterned metal layer provided over said insulating layer, wherein said electropolished metal layer has a thickness of approximately 50 to 300 Angstroms." Amended independent claim 29 also recites that "a top surface of said electropolished metal layer is electropolished down to said insulating layer."

Amended independent claim 36 recites a "memory cell" comprising *inter alia* "an electropolished patterned metal layer provided over a substrate, said electropolished metal layer having a thickness of approximately 50 to 300 Angstroms" and "a container capacitor including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode." Amended independent claim 44 recites a "processor-based system" comprising *inter alia* "a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms."

Dornfest discloses a semiconductor memory device including a bottom layer, an upper interface layer and an intermediate tuning layer between the bottom layer and upper interface layer. The interface layer of Dornfest is composed of platinum and is applied using pressure vapor deposition.

The subject matter of claims 29-32, 34-39, 41, 44-47 and 49-54 would not have been obvious over Dornfest. Dornfest fails to teach or suggest "an electropolished patterned metal layer provided over said insulating layer, wherein said electropolished metal layer has a thickness of approximately 50 to 300 Angstroms," much less "an electropolished patterned metal layer" wherein "a top surface of said electropolished metal layer is

electropolished down to said insulating layer," as amended independent claim 29 recites. Dornfest also fails to teach or suggest a "memory cell" comprising "an electropolished patterned metal layer . . . having a thickness of approximately 50 to 300 Angstroms" and "a container capacitor including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode," as amended independent claim 36 recites. Finally, Dornfest does not teach or suggest a "a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms" and as part of a "processor-based system," as amended independent claim 44 recites. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 29-32, 34-39, 41, 44-47 and 49-54 under 35 U.S.C. § 103(a) is respectfully requested.

Claims 29-32, 35-39, 45-47 and 50 stand rejected under 35 U.S.C. § 103(a) over Aoki et al. (U.S. Patent No. 6,033,953) ("Aoki"). This rejection is respectfully traversed.

Aoki relates to a "dielectric capacitor . . . which has a reduced leakage current." (Title; Abstract). According to Aoki, "[t]he surface of a first electrode (38) of the capacitor is electropolished and a dielectric film (40) and a second electrode (37) are successively laminated on it." (Abstract). Aoki emphasizes that "[t]he convex parts pointed end (38a) existing on the surface of the first electrode is very finely polished uniformly by dissolving according to electropolishing, a spherical curved surface in which the radius of curvature has been enlarged is formed, and the surface of the first electrode is flattened." (Abstract).

Aoki fails to teach or suggest all limitations of amended independent claims 29, 36 and 44. Aoki fails to teach or suggest "an electropolished patterned metal layer provided over said insulating layer" wherein "a top surface of said electropolished metal layer is electropolished down to said insulating layer," as amended independent claim 29 recites. Aoki teaches electropolishing of an *already patterned* metal layer so that "[t]he convex parts pointed end (38a) existing on the surface of the first electrode" are "very

finely polished," and not a metal layer which is patterned by electropolishing, that is "an electropolished patterned metal layer," as in the claimed invention.

Aoki also fails to teach or suggest a "memory cell" comprising "an electropolished patterned metal layer . . . having a thickness of approximately 50 to 300 Angstroms" and "a *container capacitor* including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode," as amended independent claim 36 recites. Aoki teaches a *planar* capacitor with its lower electrode subjected to a "flattening" process, and not to a *container* capacitor with its lower electrode comprised of an "electropolished patterned metal layer," as amended independent claim 36 recites. Finally, Aoki does not teach or suggest a "a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms" and as part of a "processor-based system," as amended independent claim 44 recites. For at least these reasons, the subject matter of claims 29-32, 35-39, 45-47 and 50 would not have been obvious over Aoki, and withdrawal of the rejection of these claims is respectfully requested.

Claims 29-32, 34-39, 41, 44-47 and 49-50 stand rejected under 35 U.S.C. § 103(a) over Okutoh et al. (U.S. Patent No. 6,201,271) ("Okutoh"). This rejection is respectfully traversed.

Okutoh discloses a memory device a capacitor with an upper electrode comprised of platinum and rhodium where the upper electrode is in direct contact with a surface of a ferroelectric or highly dielectric film.

The subject matter of claims 29-32, 34-39, 41, 44-47 and 49-50 would not have been obvious over Okutoh. Again, the Office Action fails to establish a *prima facie* case of obviousness. Not all claim limitations of amended independent claims 29, 36 and 44 are taught or suggested by Okutoh. Okutoh fails to teach or suggest "an electropolished patterned metal layer" having "a thickness of approximately 50 to 300 Angstroms," much less "an electropolished patterned metal layer" wherein "a top surface

of said electropolished metal layer is electropolished down to said insulating layer," as amended independent claim 29 recites. Okutoh also fails to teach or suggest a "memory cell" comprising "an electropolished patterned metal layer . . . having a thickness of approximately 50 to 300 Angstroms" and "a container capacitor including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode," as amended independent claim 36 recites. Finally, Okutoh does not teach or suggest a "a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms" and as part of a "processor-based system," as amended independent claim 44 recites. Accordingly, withdrawal of the rejection of claims 29-32, 34-39, 41, 44-47 and 49-50 under 35 U.S.C. § 103(a) is respectfully requested.

New claims 55-64 also define patentable aspects of the invention which are neither anticipated by nor rendered obvious from the references of record.

A marked-up version of the changes made to the claims by the current amendment is attached. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this

application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

A semiconductor device comprising:

a substrate;

an insulating layer provided over said substrate; and

an electropolished patterned metal layer provided over said [substrate] insulating layer, wherein said electropolished metal layer [having] has a thickness of approximately 50 to 300 Angstroms and wherein a top surface of said electropolished metal layer is electropolished down to said insulating layer.

36. (Amended) A memory cell comprising:

an electropolished patterned metal layer provided over a substrate, said electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms;

a transistor including a gate fabricated on said semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate; and

a container capacitor including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode.

44. (Amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer [provided over a

substrate, said electropolished metal layer] having a thickness of approximately 50 to 300 Angstroms.